In the Claims:

Claims 1-15 are pending.

Claims 7-12 are cancelled herein.

Claims 16-21 are newly added.

Claims 1-5 remain unchanged.

Claim 5 is amended herein.

The status of the claims is as follows:

1. (Original) A method for testing memories with seamless data input/output by interleaving seamless bank commands, comprising the steps of:

transferring data to data input/output (I/O) pins of a memory seamlessly; and

inputting control commands to control pins of the memory seamlessly.

2. (Original) The method as claimed in claim 1, wherein the data transferring step, the data are seamlessly inputted to and outputted from the input/output (I/O) pins of the memory.

3. (Original) The method as claimed in claim 1, wherein in the data transferring step, the data are seamlessly inputted into the input/output (I/O) pins of the memory.

4. (Original) The method as claimed in claim 1, wherein in the data transferring step, the data are seamlessly outputted from the input/output (I/O) pins of the memory.

5. (Original) The method as claimed in claim 1, wherein the memory has at least two banks that have the control pins for receiving the control commands.

6. (Currently amended) The method as claimed in claim 1, wherein the memory is ~~a~~ an SDRAM, DDR-DRAM or Rambus RDRAM.

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Cancelled)

15. (Cancelled)

16. (New) A method for testing memories with seamless data input/output, the method comprising the acts of:

transferring data to data input/output (I/O) pins of a memory seamlessly; and

inputting control commands to control pins of the memory, wherein said control commands to the control pins of said memory are partly delayed.

17. (New) The method as claimed in claim 16, wherein the memory has at least two banks that have the control pins for receiving the control commands.

18. (New) The method as claimed in claim 17, wherein the memory is an SDRAM, DDR-DRAM or Rambus RDRAM.

19. (New) A method for testing memories with seamless control commands, the method comprising the acts of:

transferring data to data input/output (I/O) pins of a memory, wherein the data transferred to the data input/output pins of said memory are partly masked to purposely achieve a non-seamless status; and

inputting control commands to control pins of the memory seamlessly.

20. (New) The method as claimed in claim 19, wherein the memory has at least two banks that have the control pins for receiving the control commands.

21. (New) The method as claimed in claim 19, wherein the memory is an SDRAM, DDR-DRAM or Rambus RDRAM.